CLAIMS in FWC of Serial No. 07/636,246

1. (Amended) An arrangement comprising:

a source operative to provide a DC voltage at a pair of DC terminals;

inverter means connected with the DC terminals and operative to provide an inverter voltage at a pair of inverter terminals; the inverter voltage being characterized by: (i) alternating periodically at a fundamental inverter frequency; (ii) having a fundamental period; (iii) during each fundamental period, existing for a first period at a first substantially constant voltage level and for a second period at a second substantially constant voltage level; (iv) the duration of the first period being substantially equal to that of the second period; (v) the duration of the first period being longer than one eighth [fourth] of the duration of the fundamental period; and (vi) the duration of the first period being substantively shorter than half of the duration of the fundamental period; and

load means connected with the inverter terminals and operative to draw a load current therefrom; the load means including an energy-storing inductor means and a gas discharge device.

2. The arrangement of claim 1 wherein the duration of the first period is shorter than half of the duration of the fundamental period by at least one tenth.

3. The arrangement of claim 1 wherein: (i) the duration of half the fundamental period is between 8 and 32 micro-seconds; and (ii) the duration of the first period is shorter than half of the fundamental period by at least 2 micro-seconds.

4. The arrangement of claim 1 wherein the inverter means includes at least one periodically conducting transistor.

5. (Amended) The arrangement of claim 4 wherein, during each fundamental period, the periodically conducting transistor conducts in a forward direction only during [for] a first conduction period; the first conduction period having a duration substantially shorter than the duration of the first period.

6. The arrangement of claim 5 wherein the periodically conducting transistor: (i) has an emitter and a collector; and (ii) when it indeed conducts in its forward direction, it conducts current directly between its emitter and collector without causing any substantial voltage drop thereacross.

7. The arrangement of claim 5 wherein, during each fundamental period, the period during which the periodically conducting transistor conducts in its forward direction is shorter than the first period by at least 2 micro-seconds.

8. The arrangement of claim 5 wherein: (i) each fundamental period includes a first transition period during which the inverter voltage changes from its first substantially constant voltage level to its second substantially constant voltage level; (ii) the periodically conducting transistor conducts in its forward direction during part of the first period; and (iii) the periodically conducting transistor does not conduct in its forward direction during most of the first transition period.

9. The arrangement of claim 1 wherein the inverter voltage changes between the first voltage level and the second voltage level at a substantially uniform rate.

10. The arrangement of claim 1 wherein the load means additionally includes a capacitor means connected across the inverter terminals.

11. (Amended) An arrangement comprising:

a source operative to provide a DC voltage at a pair of DC terminals;

inverter means connected with the DC terminals and operative to provide an inverter voltage at a pair of inverter terminals; the inverter means having at least one periodically conducting transistor; the inverter voltage being characterized by: (i) alternating periodically at a fundamental inverter frequency; (ii) having a fundamental period; (iii) during each fundamental period, existing for a first period at a first substantially constant voltage level and for a second period at a second substantially constant voltage level; (iv) the duration of the first period being substantially equal to that of the second period; (v) the duration of the first period being longer than one <u>eighth</u> [fourth] of the duration of the fundamental period; and (vi) the duration of the first period being shorter than half the duration of the fundamental period; and

load means connected with the inverter terminals and operative to draw a load current therefrom; the load means including an energy-storing inductor means and a gas discharge device; the load current flowing though the transistor, but only during a part of the first period.

12. (Amended) An arrangement comprising:

a source operative to provide a DC voltage at a pair of DC terminals;

inverter means connected with the DC terminals and operative to provide an inverter voltage at a pair of inverter terminals; the inverter voltage being characterized by: (i) alternating periodically at a fundamental inverter frequency, (ii) having a fundamental period, (iii) during each fundamental period, existing for a first period at a first substantially constant voltage level and for a second period at a second substantially constant voltage level, (iv) the duration of the first period being substantially equal to that of the second period, (v) the duration of the first period being longer than one eighth [fourth] of the duration of the fundamental period, and (vi) the duration of the first period being shorter than half the duration of the fundamental period; the inverter means including a periodically conducting transistor, which conducts current in its forward direction only during part of the first period; and

load means connected with the inverter terminals and operative to draw a load current therefrom; the load means including an energy-storing inductor means and a gas discharge device.

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13. An arrangement comprising:

a source operative to provide a DC voltage at a pair of DC terminals;

inverter means connected with the DC terminals and operative to provide an inverter voltage at a pair of inverter terminals; the inverter voltage having a fundamental period; the inverter means having a first periodically conducting transistor operative to conduct in its forward direction only during a first conduction period; the first conduction period having a duration substantially shorter than half the duration of the fundamental period; and

load means connected with the inverter terminals and operative to draw a load current therefrom; the load means including energy-storing inductor means and a gas discharge lamp.

14. The arrangement of claim 13 wherein the inverter means has a second alternatingly conducting transistor operative to conduct in its forward direction only during a second conduction period; the second conduction period having a duration substantially shorter than half the duration of the fundamental period.

15. The arrangement of claim 13 wherein the first conduction period has a duration shorter than one quarter of the duration of the fundamental period.

16. An arrangement comprising:

a source operative to provide a DC voltage at a pair of DC terminals;

inverter means connected with the DC terminals and operative to provide an inverter voltage at a pair of inverter terminals; the inverter voltage having a fundamental period; the inverter means having a periodically conducting transistor; the transistor having a control terminal receptive of a control signal; the control signal being an alternating voltage operative during all of a first part of each fundamental period to cause the transistor to be conductive while during all of the remainder of each such fundamental period to cause the transistor to be non-conductive; the duration of the first part being substantially shorter than half the duration of the fundamental period; and

load means connected with the inverter terminals and operative to draw a load current therefrom; the load means including energy-storing inductor means and a gas discharge lamp.

17. The arrangement of claim 16 wherein the duration of the first part is about equal to or shorter than one fourth of of the duration of the fundamental period.

18. The arrangement of claim 16 wherein the inverter means includes a pair of transistors series-connected across the DC terminals.

19. The arrangement of claim 16 wherein a shunt diode is connected in parallel with the transistor.

20. The arrangement of claim 16 including means for controlling the duration of said first part.